What is claimed is:

1. A method of forming a gate oxide on a transistor body region, comprising:

evaporation depositing a metal layer on the body region, the metal being chosen from a group consisting of the group IIIB elements and the rare earth series of the periodic table; and

oxidizing the metal layer to form a metal oxide layer on the body region.

2. The method of claim 1, wherein evaporation depositing the metal layer includes depositing a metal layer, the metal layer being chosen from a group consisting of yttrium and gadolinium.

3. The method of claim 1, wherein evaporation depositing the metal layer includes evaporation depositing by electron beam evaporation.

4. The method of claim 3, wherein electron beam evaporation depositing the metal layer includes electron beam evaporation of a 99.9999% pure metal target material.

5. The method of claim 1, wherein evaporation depositing the metal layer includes evaporation depositing at a substrate temperature of approximately 150 - 400 °C.

6. The method of claim 1, wherein oxidizing the metal layer includes oxidizing at a temperature of approximately 400 °C.

7. The method of claim 1, wherein oxidizing the metal layer includes oxidizing with atomic oxygen.

8. The method of claim 1, wherein oxidizing the metal layer includes oxidizing using a krypton (Kr)/oxygen (O_2) mixed plasma process.

9. A method of forming a gate oxide on a transistor body region, comprising:

evaporation depositing a metal layer on the body region, the metal being chosen from a group consisting of the group IIIB elements and the rare earth series of the periodic table; and

oxidizing the metal layer using a krypton(Kr)/oxygen (O_2) mixed plasma process to form a metal oxide layer on the body region.

10. The method of claim 9, wherein evaporation depositing the metal layer includes depositing a metal layer, the metal layer being chosen from a group consisting of yttrium and gadolinium.

11. The method of claim 9, wherein evaporation depositing the metal layer includes evaporation depositing by electron beam evaporation.

12. The method of claim 11, wherein electron beam evaporation depositing the metal layer includes electron beam evaporation of a 99.9999% pure metal target material.

13. The method of claim 9, wherein evaporation depositing the metal layer includes evaporation depositing at a substrate temperature of approximately 150 - 400 °C.

14. A method of forming a transistor, comprising:

forming first and second source/drain regions;

forming a body region between the first and second source/drain regions;

evaporation depositing a metal layer on the body region, the metal being chosen from a group consisting of the group IIIB elements and the rare earth series of the periodic table;

oxidizing the metal layer to form a metal oxide layer on the body region; and

coupling a gate to the metal oxide layer.

15. The method of claim 14, wherein evaporation depositing the metal layer includes depositing a metal layer, the metal layer being chosen from a group consisting of yttrium and gadolinium.

16. The method of claim 14, wherein evaporation depositing the metal layer includes evaporation depositing by electron beam evaporation.

17. The method of claim 16, wherein electron beam evaporation depositing the metal layer includes electron beam evaporation of a 99.9999% pure metal target material.

18. The method of claim 14, wherein evaporation depositing the metal layer includes evaporation depositing at a substrate temperature of approximately 150 - 400 °C.

19. The method of claim 14, wherein oxidizing the metal layer includes oxidizing at a temperature of approximately 400 °C.

20. The method of claim 14, wherein oxidizing the metal layer includes oxidizing with atomic oxygen.

21. The method of claim 14, wherein oxidizing the metal layer includes oxidizing using a krypton (Kr)/oxygen (O_2) mixed plasma process.

22. A method of forming a memory array, comprising:

forming a number of access transistors, including:

forming first and second source/drain regions;

forming a body region between the first and second source/drain regions;

evaporation depositing a metal layer on the body region, the metal being chosen from a group consisting of the group IIIB elements and the rare earth series of the periodic table;

oxidizing the metal layer to form a metal oxide layer on the body region;

coupling a gate to the metal oxide layer;

forming a number of wordlines coupled to a number of the gates of the number of access transistors;

forming a number of sourcelines coupled to a number of the first source/drain regions of the number of access transistors; and

forming a number of bitlines coupled to a number of the second source/drain regions of the number of access transistors.

23. The method of claim 22, wherein evaporation depositing the metal layer includes depositing a metal layer, the metal layer being chosen from a group consisting of yttrium and gadolinium.

24. The method of claim 22, wherein evaporation depositing the metal layer includes evaporation depositing by electron beam evaporation.

25. The method of claim 24, wherein electron beam evaporation depositing the metal layer includes electron beam evaporation of a 99.9999% pure metal target material.

26. The method of claim 22, wherein evaporation depositing the metal layer includes evaporation depositing at a substrate temperature of approximately 150 - 400 °C.

27. The method of claim 22, wherein oxidizing the metal layer includes oxidizing at a temperature of approximately 400 °C.

28. The method of claim 22, wherein oxidizing the metal layer includes oxidizing with atomic oxygen.

29. The method of claim 22, wherein oxidizing the metal layer includes oxidizing using a krypton (Kr)/oxygen (O_2) mixed plasma process.

30. A transistor, comprising:

a first and second source/drain region;

a body region located between the first and second source/drain regions, wherein a surface portion of the body region has a surface roughness of approximately 0.6 nm;

a yttrium oxide dielectric layer coupled to the surface portion of the body region; and

a gate coupled to the yttrium oxide dielectric layer.

31. The transistor of claim 30, wherein the yttrium oxide dielectric layer includes Y_2O_3.

32. The transistor of claim 30, wherein the surface portion of the body region is oriented in the (100) crystalline plane.

33. The transistor of claim 30, wherein the surface portion of the body region is oriented in the (111) crystalline plane.

34. The transistor of claim 30, wherein the yttrium oxide dielectric layer is substantially amorphous.

35. The transistor of claim 30, wherein the yttrium oxide dielectric layer is partially crystalline.

36. A transistor, comprising:

a first and second source/drain region;

a body region located between the first and second source/drain regions, wherein a surface portion of the body region has a surface roughness of approximately 0.6 nm;

a gadolinium oxide dielectric layer coupled to the surface portion of the body region; and

a gate coupled to the gadolinium oxide dielectric layer.

37. The transistor of claim 36, wherein the gadolinium oxide dielectric layer includes Gd_2O_3.

38. The transistor of claim 36, wherein the surface portion of the body region is oriented in the (100) crystalline plane.

39. The transistor of claim 36, wherein the surface portion of the body region is oriented in the (111) crystalline plane.

40. The transistor of claim 36, wherein the yttrium oxide dielectric layer is substantially amorphous.

41. The transistor of claim 36, wherein the yttrium oxide dielectric layer is partially crystalline.

42. A memory array, comprising:

a number of access transistors, including:

a first and second source/drain region;

a body region located between the first and second source/drain regions, wherein a surface portion of the body region has a surface roughness of approximately 0.6 nm;

a yttrium oxide dielectric layer coupled to the surface portion of the body region;

a gate coupled to the yttrium oxide dielectric layer;

a number of wordlines coupled to a number of the gates of the number of access transistors;

a number of sourcelines coupled to a number of the first source/drain regions of the number of access transistors; and

a number of bitlines coupled to a number of the second source/drain regions of the number of access transistors.

43. The memory array of claim 42, wherein the yttrium oxide dielectric layer includes Y_2O_3.

44. The memory array of claim 42, wherein the yttrium oxide dielectric layer exhibits a dielectric constant (k) of approximately 18.

45. The memory array of claim 42, wherein the yttrium oxide dielectric layer exhibits a conduction band offset greater than approximately 2 eV.

46. The memory array of claim 42, wherein the yttrium oxide dielectric layer is substantially amorphous.

47. The memory array of claim 42, wherein the yttrium oxide dielectric layer is partially crystalline.

48. A memory array, comprising:

a number of access transistors, including:

a first and second source/drain region;

a body region located between the first and second source/drain regions, wherein a surface portion of the body region has a surface roughness of approximately 0.6 nm;

a gadolinium oxide dielectric layer coupled to the surface portion of the body region;

a gate coupled to the gadolinium oxide dielectric layer;

a number of wordlines coupled to a number of the gates of the number of access transistors;

a number of sourcelines coupled to a number of the first source/drain regions of the number of access transistors; and

a number of bitlines coupled to a number of the second source/drain regions of the number of access transistors.

49. The memory array of claim 48, wherein the gadolinium oxide dielectric layer includes Gd_2O_3.

50. The memory array of claim 48, wherein the gadolinium oxide dielectric layer exhibits a dielectric constant (k) of approximately 14.

51. The memory array of claim 48, wherein the gadolinium oxide dielectric layer exhibits a conduction band offset greater than approximately 2 eV.

52. The memory array of claim 48, wherein the yttrium oxide dielectric layer is substantially amorphous.

53. The memory array of claim 48, wherein the yttrium oxide dielectric layer is partially crystalline.

54. A transistor formed by the process, comprising:

forming a body region coupled between a first source/drain region and a second source/drain region;

evaporation depositing a metal layer on the body region, the metal being chosen from a group consisting of the group IIIB elements and the rare earth series of the periodic table;

oxidizing the metal layer to form a metal oxide layer on the body region; and

coupling a gate to the metal oxide layer.

55. The transistor of claim 54, wherein evaporation depositing the metal layer includes depositing a metal layer, the metal layer being chosen from a group consisting of yttrium and gadolinium.

56. The transistor of claim 54, wherein evaporation depositing the metal layer includes evaporation depositing by electron beam evaporation.

57. The method of claim 54, wherein oxidizing the metal layer includes oxidizing using a krypton (Kr)/oxygen (O_2) mixed plasma process.

58. A method of forming an information handling system, comprising:

forming a processor;

forming a memory array, including:

forming a number of access transistors, including:

forming first and second source/drain regions;

forming a body region between the first and second source/drain regions;

evaporation depositing a metal layer on the body region, the metal being chosen from a group consisting of the group IIIB elements and the rare earth series of the periodic table;

oxidizing the metal layer to form a metal oxide layer on the body region;

coupling a gate to the metal oxide layer;

forming a number of wordlines coupled to a number of the gates of the number of access transistors;

forming a number of sourcelines coupled to a number of the first source/drain regions of the number of access transistors;

forming a number of bitlines coupled to a number of the second source/drain regions of the number of access transistors; and

forming a system bus that couples the processor to the memory array.

59. The method of claim 58, wherein evaporation depositing the metal layer includes depositing a metal layer, the metal layer being chosen from a group consisting of yttrium and gadolinium.

60. The method of claim 58, wherein evaporation depositing the metal layer includes evaporation depositing by electron beam evaporation.

61. An information handling device, comprising:

a processor;

a memory array, comprising:

a number of access transistors, comprising:

a first and second source/drain region;

a body region located between the first and second source/drain regions, wherein a surface portion of the body region has a surface roughness of approximately 0.6 nm;

a yttrium oxide dielectric layer coupled to the surface portion of the body region;

a gate coupled to the yttrium oxide dielectric layer;

a number of wordlines coupled to a number of the gates of the number of access transistors;

a number of sourcelines coupled to a number of the first source/drain regions of the number of access transistors;

a number of bitlines coupled to a number of the second source/drain regions of the number of access transistors; and

a system bus coupling the processor to the memory device.

62. The information handling device of claim 61, wherein the yttrium oxide dielectric layer exhibits a dielectric constant (k) of approximately 18.

63. The information handling device of claim 61, wherein the yttrium oxide dielectric layer is substantially amorphous.

64. An information handling device, comprising:

a processor;

a memory array, comprising:

a number of access transistors, comprising:

a first and second source/drain region;

a body region located between the first and second source/drain regions, wherein a surface portion of the body region has a surface roughness of approximately 0.6 nm;

a gadolinium oxide dielectric layer coupled to the surface portion of the body region;

a gate coupled to the gadolinium oxide dielectric layer;

a number of wordlines coupled to a number of the gates of the number of access transistors;

a number of sourcelines coupled to a number of the first source/drain regions of the number of access transistors;

a number of bitlines coupled to a number of the second source/drain regions of the number of access transistors; and

a system bus coupling the processor to the memory device.

65. The information handling device of claim 64, wherein the gadolinium oxide dielectric layer exhibits a dielectric constant (k) of approximately 14.

66. The information handling device of claim 64, wherein the gadolinium oxide dielectric layer is substantially amorphous.